REMARKS

The following remarks are made in response to the Final Office Action mailed December 4, 2008, and the Advisory Action mailed March 20, 2009. Claims 20-31 have been withdrawn from consideration. Claims 1-13 have been cancelled. With this Response, claims 14-16 and 32 have been amended. Claims 14-19, 32 and 33 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 14, 18-19 and 32 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Yamamoto et al. (US Publ. 2003/0094675 "Yamamoto") in view of Ohta et al. (US 6,379,998 "Ohta"). Applicants respectfully traverse these rejections.

To establish *prima facie* obviousness, all claim limitations must be considered. MPEP 2143.03 (citing *In re Wilson*, 424 F.2d 1382, 1385, (CCPA 1970). The Office Action admits that Yamamoto fails to disclose each claim element. More specifically, the Office Action admits, "Yamamoto et al. do not disclose the active top of the sensor chip and the plastic plate having a planar overall top side." Office Action at p. 3.

Independent claims 14 and 32 each further include, "the active top side of the sensor chip *and top sides of the contact areas*, together with a top side of the plastic plate having a planar overall top side." The Office Action further fails to identify a teaching or suggestion in Yamamoto of top sides of contact areas forming a planar overall top side with the active top of the sensor chip and the plastic plate. In response to this argument, the Advisory Action states. "Ohta discloses this feature. Ohta discloses a sensor chip 33 is embedded in substrate 31 and is co-planar with the substrate (Ohta fig. 26)."

However the Advisory Action failed to address the recitation in the claims of *top sides of the contact areas* together with the top sides of the sensor chip and plastic plate having a planar overall top side. Instead, the Advisory Action merely says a chip is embedded in a substrate.

Moreover, claims 14 and 32 each include external contact areas situated on the top side of the plastic plate, and claim 14 recites

> "a rewiring structure with a rewiring layer having flat rewiring lines extending from the contact areas to the external contact areas, the flat rewiring lines being arranged on the planar overall top side such that the flat rewiring lines extend in a common plane, and are positioned directly on portions of the active top side of the sensor chip and the top side of the plastic plate."

Claim 32 is presented in "means-plus-function" language as provided by 35 USC 112, sixth paragraph. As such, the claim should be interpreted in view of the structure disclosed that corresponds to the "means" associated with the recited function. *See, In re Donaldson*, 16 F.3d 1189, 29 USPQ2d 1845 (Fed. Cir. 1994). Thus, the means for connecting the contact areas to the external contact areas of the sensor components includes a rewiring structure with a rewiring layer having flat rewiring lines arranged on the planar overall top side that extend in a common plane and are positioned directly on portions of the active top side of the sensor chip and the top side of the plastic plate as disclosed in the drawings and written description of the present application.

The Office Action fails to identify a disclosure in either Yamamoto or Ohta of the claimed rewiring structure. The Office Action appears to equate the leads 2 disclosed in Yamamoto (for example, shown in Figure 1B of Yamamoto) to the external contacts recited in the claims. The leads 2, however, appear to be embedded in the package 3 in Yamamoto – not on the top side of the package. The Office Action fails to identify external contacts in Ohta, but rather, simply points out that the top side of the chip 33a is co-planar with the top side of the substrate 31.

Thus, the cited portions of Yamamoto and Ohta, either alone or in combination, fail to disclose each claim limitation of claim 14 and 32.

Moreover, it is well settled that, to establish *prima facie* obviousness, there must be motivation to the disclosure of a prior art reference using the teachings of another reference. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. MPEP 2143.01 (citing *In re Gordon*, 733 F.2d 900 (Fed. Cir. 1984).

Yamamoto is directed to a package including guide projections and spring projections to provide accuracy in mounting and positioning a semiconductor chip onto a package. *See* Yamamoto at abstract. Figure 2 of Yamamoto is reproduced below.

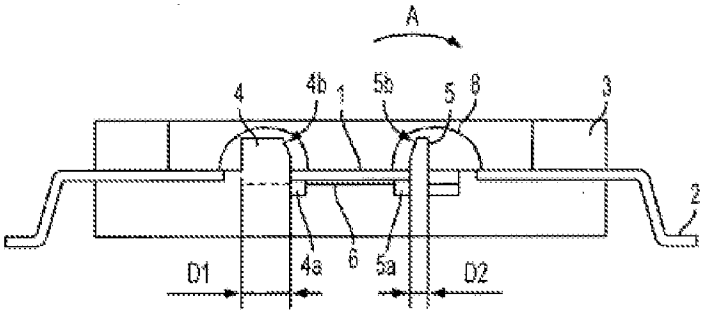

FIG. 2

Figure 2 of Yamamoto illustrates the package 3 including guide projections and spring projections 4 and 5, which extend well above the top surface of the chip 1, presumably, to facilitate receiving and positioning the chip 1. If Yamamoto is modified as suggested in the Office Action, to make the top surfaces of the chip 1 and package 3 co-planar, the guide and spring projections 4 and 5 would not extend beyond the top surface and therefore would not function satisfactorily.

Thus, the Office Action fails to establish prima facie obviousness of independent claims 14 and 32, as well as claims 18 and 19 which depend from claim 14. Claims 14, 18, 19 and 32 are thus believed to be in condition for allowance.

Still further, Yamamoto discloses a leaded package for sensor components that, as admitted in the Office Action, does not include active top side of the sensor chip and top sides of the contact areas, together with a top side of the plastic plate having a planar overall top side. The Office Action refers to the disclosure of Ohta, saying the substrate and embedded chip of Ohta form "a smooth flattening layer permitting the wiring be made easily. Office Action at p. 3 (citing Ohta col. 24, ll. 15-29)

The cited portion of Ohta describes the structure illustrated in Figure 56 thereof, and reads as follows, "Also when a level difference occurs between the embedded chip 52 and the body chip 53, the flattening layer 60 can smooth the level difference, thus permitting the wirings to be surely made."

Ohta discloses an arrangement in which a semiconductor chip is arranged in an etched indentation in a silicon substrate. Figure 59 illustrates "a flattening layer 60 [that] may be made of a spin-on-glass (SOG) film." Ohta at col. 24, ll. 1-2. Such materials are typically used as materials for the dielectric layer and rewiring structure on the active surface of semiconductor chips. The Ohta reference relates to semiconductor chip technology rather than packaging technology which is the technical art of the present application. The problems encountered in the two arts are quite different.

Therefore, the person of ordinary skill in the art would not have considered the arrangement of the flattening layer in a semiconductor chip technology to be of technical relevance to the problem of packaging a sensor component.

Even if the person of ordinary skill in the art had considered the Ohta reference, a combination of the two references fails to lead to the arrangement of the claims. Ohta teaches a flattening layer 60 for bridging a gap which occurs between the first semiconductor chip and the semiconductor substrate. However, such a gap fails to occur in the arrangement of the present application as the chip is embedded in plastic. Therefore, the person of ordinary skill in the art would not have seen a use for the flattening layer of Ohta when looking to modify the arrangement of Yamamoto since there is no gap to bridge.

Furthermore, it is also not obvious to modify the package of Yamamoto to include rewiring lines that extend in a plane and are positioned directly on top of the semiconductor chip and plastic plate in which the semiconductor chip is embedded. Silicon and plastic have very different thermal expansion coefficients. Therefore, it would not be obvious for the person of ordinary skill in the art that an arrangement in which the rewiring lines are positioned directly on the semiconductor chip as well as the plastic plate would function, since he would expect the

rewiring lines to fail due to this difference in the thermal expansion coefficients of silicon and plastic.

For at least these reasons, Applicants respectfully submit that claims 14 and 32 are patentable over the combination of Yamamoto and Ohta. Claims 18 and 19 depend on claim 14 and are therefore allowable for at least the same reasons.

Claims 15-17 and 33 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Yamamoto and Ohta, and further in view of Fillion et al. (US 5,353,498). Claims 15-17 and 33 all ultimately depend from either claim 14 or claim 32, which are allowable as set forth above. Claims 15-17 and 33 are therefore allowable for at least the same reasons.

CONCLUSION

In view of the above, Applicant respectfully submits that all of the pending claims are in form for allowance. Therefore, reconsideration and withdrawal of the rejections and allowance of claims are respectfully requested.

Applicant hereby authorizes the Commissioner for Patents to charge Deposit Account No. 50-0471 in the amount of $130.00 to cover the fees as set forth under 37 C.F.R. 1.16(h)(i).

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Mark L. Gleason at Telephone No. (612) 767-2503, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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